User's Guide
SLWU063F–April 2009–Revised April 2011

GC5325 System Evaluation Kit

This document outlines the basic steps and functions that are required to ensure the proper operation of the GC5325 System Evaluation Kit (SEK) system. The GC5325 is a fully integrated crest-factor reduction (CFR), digital predistortion (DPD) device capable of linearizing a typical base-station power amplifier (PA). This guide can help users to quickly evaluate the performance of various PAs with varying system parameters, such as CFR levels and PA input/output power levels before and after the DPD. The GC5325 EVM has two GC5325 devices configured to provide two separate transmit paths and uses one ADC for feedback that is shared by both GC5325 parts. The block diagram for the GC5325SEK is shown Figure 1.

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1 Overview

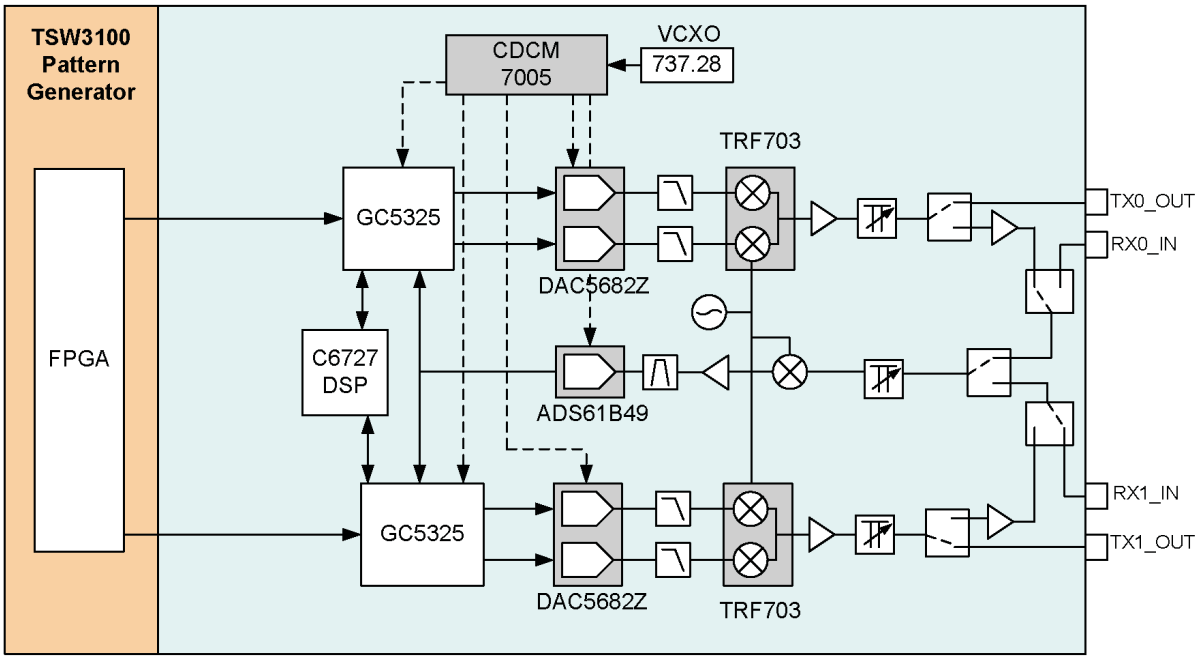

Figure 1. GC5325EVM Block Diagram

The GC5325 SEK consists of the following modules:

- GC5325EVM board (center in Figure A in the GC5325SEK Figures file on the provided CD)
- TSW3100 pattern-generator board (left in Figure A)

The digital portion of the GC5325EVM consist of two GC5325s which are used to generate the DPD corrected data for two duplicate transmit paths. The control of the GC5325's is provided by a TMS320C6727 Digital Signal Processor (DSP). The GC5325EVM communicates to a host PC via a DSP-Weuffen USB-to-UHPI interface board. The system clocking is provided by an onboard VCXO which is divided by a CDCM7005 to provide the required clocks for the two DACs, the ADC, two GC5325s, the FPGA, and the TSW3100 pattern generator. The default VCXO is 737.28 MHz, although this can be substituted with another VCXO or bypassed by using an external clock source.

The radio frequency (RF) portion of the board has two duplicated transmit paths that use a DAC5682Z (16-bit, 1-GSPS, dual-channel) and TRF3703 for the TX conversion to RF. This is followed by an amplifier, Digital Step Attenuator (DSA) , and RF switch (for optional onboard loopback to feedback path). The RF section of the board also features a shared feedback path which consists of RF switches (control shared feedback), DSA, and a mixer to convert to IF. At the intermediate frequency (IF) portion of the board is an amplifier, a filter stage, and then the ADS61B49 ADC (14-bit, 250-MSPS).

The baseband input test data is provided by the Texas Instruments TSW3100 pattern generator. This board communicates with the host PC using a USB-to-Ethernet interface. The GC5325EVM plugs directly into the TSW3100 as shown in Figure A of the GC5325SEK Figures file on the provided CD. The entire system is controlled by the GC5325 graphical user interface (GUI) software.

2 Hardware Setup

The setup procedure begins with verifying that all proper connections are made between the various components of the SEK system. The system is fully controlled by a single host personal computer (PC). The following list describes connections between the various components of the system including those to the PC:

The interconnections of various units of the GC5325SEK are as follows:

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- The composite signal input patterns used by the GC5325 are generated using the TSW3100 pattern generator. The TSW3100 is programmed through an Ethernet cable via FTP commands issued by the GC5325GUI. The TSW3100 CMOS output headers J63 and J64 connect to corresponding female 40-pin headers J1 and J3 on the bottom of the GC5325EVM. These headers provide composite signal data, baseband clock, frame strobe, and synchronization to the GC5325EVM. Align the GC5325EVM bottom connectors J1 and J3 over the top connectors J63 and J64 of the TSW3100. Ensure that all pins are aligned with the sockets. Press down on the GC5325EVM until the connectors are flush with each other.
- The TSW3100-required input CMOS clock is provided by connecting the CMOS_CLK SMA (J73) on the TSW3100 to PG_CLK_OUT SMA (J2) connector on the GC5325EVM using the provided SMA coaxial cable as shown in Figure B of the provided GC5325SEK Figures file on the provided CD. It is used for providing the reference clock from the GC5325EVM, which is derived from the YOA and YOB output of the CDCM7005 through the FPGA (dividing by 3). The frequency on GC5325 J2 must be the VCXO frequency divided by 6. With the 737.28-MHz VCXO, this output is 122.88 MHZ. Install the provided SMA coaxial cable between these connectors.
- Downloading of the DSP runtime code and control of the RF section of the card, including the clock generator (CDCM7005) is achieved through the DSP Weuffen USB-UHPI interface board, which plugs into J25 and J26 of the GC5325EVM. Plug in the provided USB cable from the mini-USB port on the small green interface board mounted on the top of the GC5325EVM in the lower left corner and to a host PC USB port
- Power to the system comes from the provided 19-Vdc power supply (Dell) through J7. An alternate method is to provide 19 Vdc to connector J23. The GC5325EVM converts the 19 Vdc down to the required voltages needed by the board as well as generate the 4.5 - 5 Vdc for the TSW3100. Connect the provided power supply to connector J7 of the GC5325EVM. Switch SW4 is the GC5325SEK main power switch.
- Power for the TSW3100 is made available from the GC5325EVM on connector J22 (PG_PWR) via the provided power cable which plugs into the power connector J9 on the TSW3100 as shown in Figure D of the GC5325SEK Figures file on the provided CD. Install the provide power cable as shown. Ensure that switch SW1 on the TSW3100 is set to the ON position, SW5 is in the OFF position and all switches on SW2 are set to the " Open" position.
- Control of the TSW3100 is through an Ethernet interface between the TSW3100 and the host PC. The GC5325SEK provides an USB-to-Ethernet adapter which allows the user to use an USB port for this interface instead of the Ethernet port, which in most cases is already being used. Connect the provided Ethernet cross over cable between the TSW3100 and the adapter. Next connect the adapter to an USB port. The GC5325SEK setup now appears as shown in Figure E of the GC5325SEK Figures file on the provided CD.
- Local oscillator (LO) inputs are located at SMA connectors J20 and J19 (see Figure 2). The board default configuration is to operate with a single LO source provided from TX_LO_IN connector (J20). Connect the external LO source to J20 and set the desired frequency. If using the high frequency configuration (default) use a power level such that the power at the input connector J20 is at approximately +2 dBm. If using the low frequency configuration, depending on the frequency selected, the LO power should be set approximately to -7 dBm to prevent signal saturation. If using an external filter (recommended) with the external LO source, any cable and filter loss must be taken into consideration.

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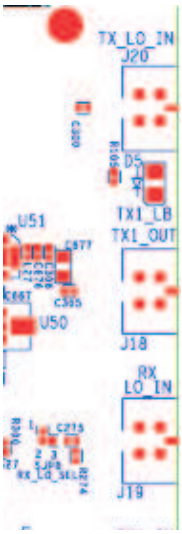

Figure 2. Location of Local Oscillator Inputs

NOTE: If a different power level is used, make sure the LO power level at both transmit modulators and the receive mixer are within the required specification. SMD coaxial connector switches are provided throughout the RF section of the GC5325EVM. Two of them can be used to measure the LO power at the transmit modulators, and one can be used to measure the power of the LO going to the receive mixers. See the schematic for the exact reference designator. The connectors normally pass the RF signal from pin 1 to pin 2 with minimal loss. When a special test cable from Murata (part no. MXGS83RK3000) is inserted into these switches, the signal path from pin 1 and pin 2 is disconnected, and the signal is then routed from pin 1 to the test cable.

- The GC5325SEK is designed to operate over two different frequency ranges: 700 to 1400 MHz and 1600 to 3000 MHz. The user must make sure the LO source frequency is set to match the configuration of the board. To support the two operating frequency ranges, the receive path contains two separate RF mixers, along with a wideband amplifier and attenuator. The GC5325EVM default configuration is with two active mixers installed. The EVM also has an option to be configured with passive mixers if desired. Jumpers JP7 and JP8 determine which mixer is used in the feedback path, while jumpers JP6 and JP9 provide power or not to the mixers. Figure 3, which is the actual silkscreen that is labeled on the top right side of the GC5325 EVM, shows how to set these jumpers per the desired mode of operation.

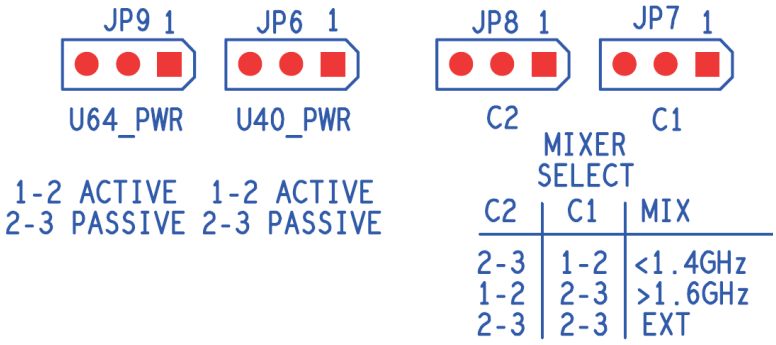

Figure 3. Mixer Jumper Definition

- Transmit (TX) outputs are located at SMA connectors J17 (TX0_OUT) and J18 (TX1_OUT). The receive (RX) inputs (feedback) are located at SMA connectors J46 (RX0_IN) and J28 (RX1_IN). The receive inputs must not exceed approximately -10 dBm. The user may need to provide an attenuator in

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the path between the PA output and GC5325 receive input signals. A typical configuration using two Mini-Circuit amplifiers, two RF couplers and the GC5325 EVM is shown in Figure F in the GC5325SEK Figures file on the provided CD.

NOTE: To avoid any significant performance degradation, TI strongly suggests the use of a RF bandpass filter to reject undesirable products in the transmitted signal. The filter must have a 1-dB bandwidth of 100 MHz to accommodate the full DPD correction bandwidth and must be used between the TX output and the PA input. Additionally, the filter must have minimum amplitude (+/-0.5 dB) and group delay variation (±2 ns) over the pass band.

- The GC5325 EVM contains two dip switch modules. The default switch settings are as follows:
  - SW5 – All switches must be set to the "Open" position.
  - SW7 - All switches must be set to the "Closed" position.

  Switches 1 and 2 of dip switch SW5 set the frequency of the PG_CLK_OUT signal on SMA J2 of the GC5325EVM. Based on the VCXO, these switches must be in the correct positions to provide the proper baseband clock frequency to the TSW3100.

VCXO Frequency	CDCM7005 DIVIDE of VCXO CLK	SW1	SW2	J2 Output Frequency
737.28 MHz	DIVIDE BY 2	OPEN	OPEN	122.88 MHz
737.28 MHz	DIVIDE BY 2	CLOSED	OPEN	147.45 MHz
737.28 MHz	DIVIDE BY 2	OPEN	CLOSED	147.45 MHz
672 MHz	DIVIDE BY 2	OPEN	OPEN	112 MHz
672 MHz	DIVIDE BY 2	CLOSED	OPEN	134.4 MHz
672 MHz	DIVIDE BY 2	OPEN	CLOSED	134.4 MHz
672 MHz	DIVIDE BY 3	OPEN	OPEN	74.6 MHz
672 MHz	DIVIDE BY 3	CLOSED	OPEN	89.6 MHz
672 MHz	DIVIDE BY 3	OPEN	CLOSED	89.6 MHz

Switch 3 of SW5 is not used. Switch 4 allows the RF section of the board to be either controlled by the DSP or the FTDI USB adapter board mounted on the bottom of the GC5325EVM. The FTDI USB driver software has not been very reliable and this interface should not be used.

2.1 Power-Up Sequence

Toggle switch SW4 on the GC5325EVM is the main power ON/OFF switch for both boards as long as SW1 on the TSW3100 is in the ON position. SW5 on the TSW3100 controls two onboard regulators that provide power to the banana jacks for optional external power. These are not used with the GC5325SEK, and SW5 should remain in the OFF position. With power applied, certain status LEDs illuminate. See Appendix A of this document for LED descriptions.

After the cables are installed and power is provided to the system, LEDs D1-D4 will display the current version of firmware that is loaded inside the FPGA, with LED D1 the LSB and LED D4 the MSB of a four-bit binary word. Both TX Channel Loop Back LEDs are illuminated (D5 and D6) along with two CDCM7005 status LEDs (D14 and D15) after power up.

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3 Software Installation

The following steps outline the installation of the software tools/utilities required to operate the SEK system. These software components (supplied with the GC5325SEK) must be installed:

- MATLAB™ control libraries and tools, to program and control the EVM system. This requires Windows™ XP SP2 and a COM port on the host PC.
- USB-Ethernet software driver (see section 2.1, *USB to Ethernet Adapter Installation* and section 2.2, *Configure the USB to Ethernet Network*, in the TSW3100 user's guide SLLU101)
- DSP-Weffen USB-to-UHPI software driver.

3.1 MATLAB™ Control Libraries and Tools

The user can begin with the installation of the MATLAB control libraries and tools. The required software is included on the provided compact disc (CD).

The following steps outline this installation:

1. Create the following directory: C:\GC5325. Copy the \GC5325EVMGUI_xpxxx (where xpxxx is the GUI version) directory from the provided CD into C:\GC5325\
2. Go to the C:\GC5325\GC5325EVMGUI_xpxxx \ directory, and click on **MCRInstaller.exe** and install the MATLAB runtime library.

3.2 TSW3100 Software and Drivers

The GC5325SEK comes with a USB-to-Ethernet adapter that can be used to communicate between a host PC USB port and the TSW3100. The software/driver installation procedure for this product can be found in the TSW3100EVM User's Guide and must be installed now if it has not already been installed. The TSW3100EVM User's Guide and software can be found under the TSW3100 directory on the provided CD.

3.3 DSP-Weuffen USB-to-UHPI Software and Driver

For the USB-UHPI software, the required device drivers are included in the C:\GC5325EVMGUI_xpxxx \DLL_drivers\ usb_UHPI directory.

The following steps outline this installation:

1. Ensure that the USB cable from the USB-UHPI EVM (small green board) on top of the GC5325EVM to the host PC USB port is installed.
2. Turn on the GC5325EVM and TSW3100 using switch SW4 on the GC5325EVM.
3. The PC automatically detects a new device. At the *New hardware installation* prompt, select *No, not at this time*.
4. Select *User specified location* for the drivers, and browse for the directory within the \GC5325EVMGUI\DLL drivers\usb_UHPI directory. Click continue.
5. Accept the driver signature and continue.

After installing the DSP-Weuffen USB-to-UHPI and the USB-to-Ethernet adapter drivers, ensure that the devices are installed by using the Control Panel/System/Hardware/Device Manager.

The installation of the software, tools, libraries, and drivers is now complete. Power should now be cycled on the EVM.

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4 Using the Software

4.1 Starting the GUI Software

To start the GC5325 GUI software installation, double click on the GC5325GUI_setup.exe file on the provide CD.

When the Setup Wizard opens, click on "Next".

Read the License Agreement and click on "I accept the agreement".

Click on "Next".

The destination folder for the installed software is displayed. TI recommends using the default folder location. All necessary folders will be created by the installation software.

Click on "Next".

Click on "Install" to start the installation.

After the installation is complete, click on "Finish".

If the default location was used, the software is now loaded under the directory called "C:\GC5325GUI".

Go to this folder and double click on the file called GC5325EVM.exe to start the GC5325 GUI.

The program usually takes about 15 seconds to start. Both a DOS window and a GUI appear. The DOS window displays useful text during operation of the GUI, equivalent to the MATLAB Command window for the uncompiled GUI. This looks as shown in Figure 4. The GUI looks as shown in Figure 5.

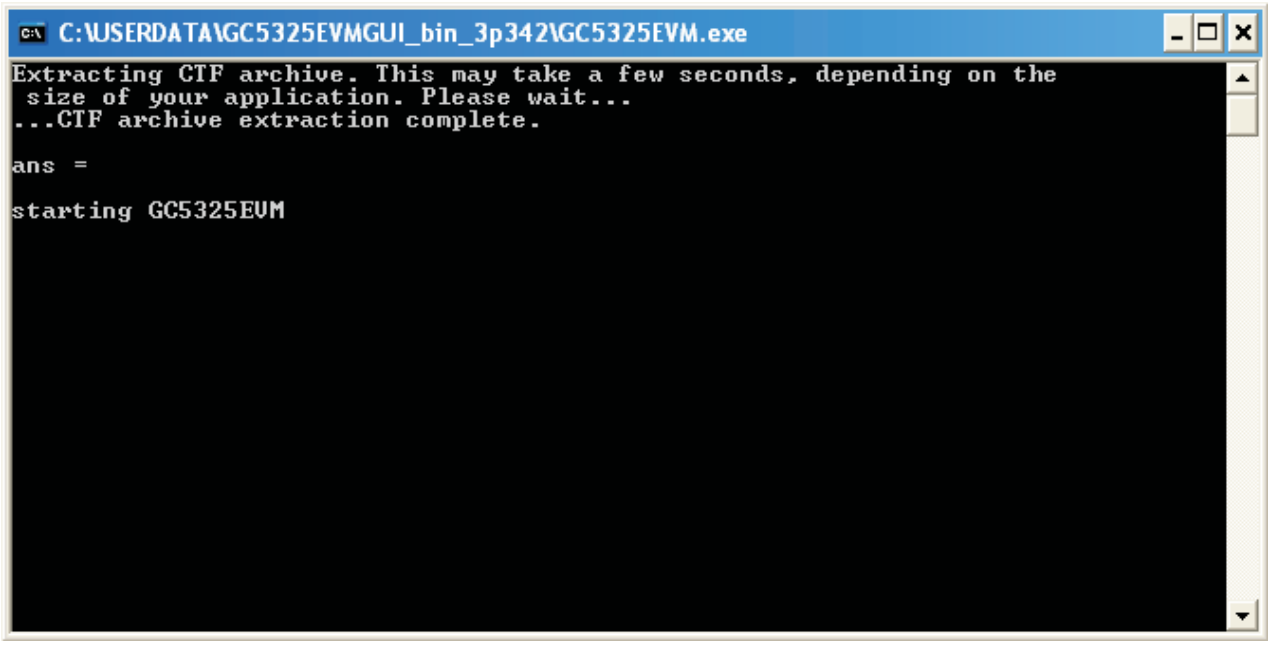

Figure 4. DOS Window at Start-Up

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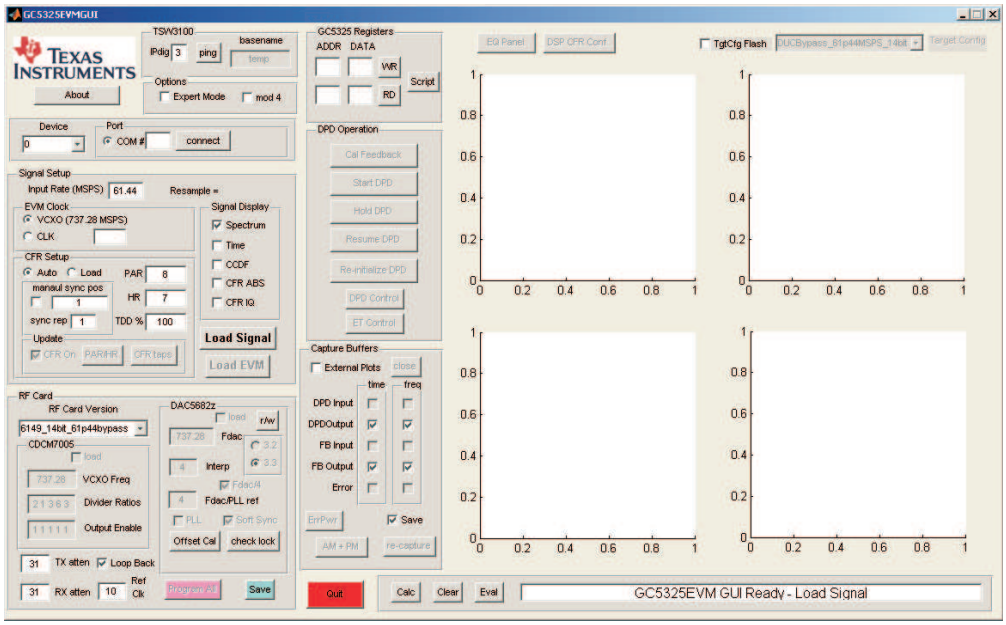

Figure 5. GUI at Start-Up

To load the DSP code through the USB-to-UHPI adapter, do the following steps:

1. In the GC5325 Registers box of the GUI, enter "5325internal" inside the ADDR box, then click on the "WR" button.

2. Select "UHPI BOOT" located in the upper right side of the GUI.

3. Select "UHPI" in the left side of the GUI.

4. Select "DSP" in the RF Port Options box located in the bottom right hand corner of the GUI. The GUI shall now appear as shown in Figure 6.

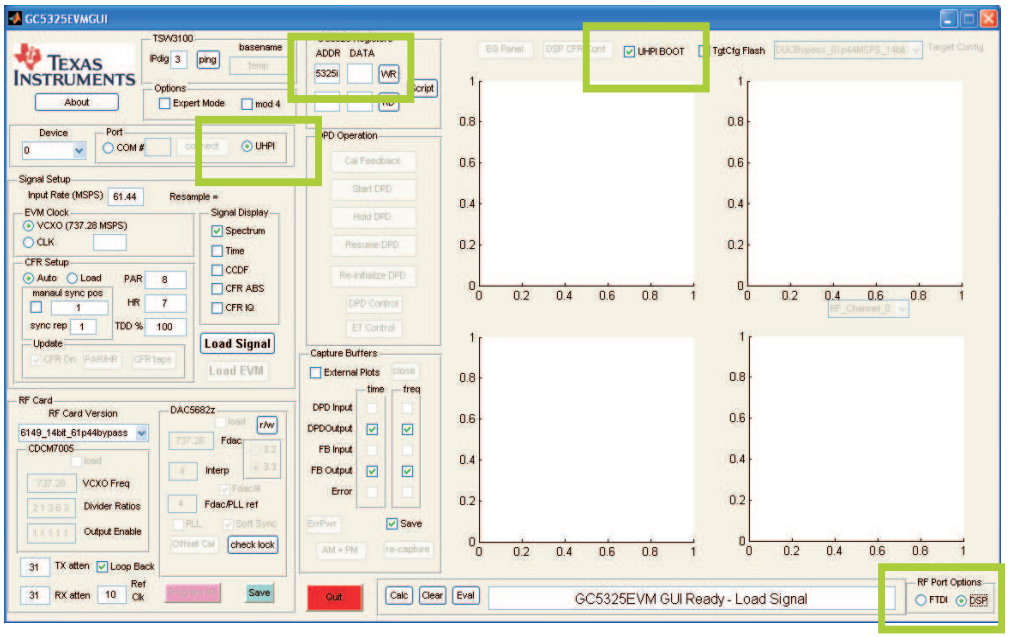

Figure 6. GUI Configured for UHPI Loading of DSP

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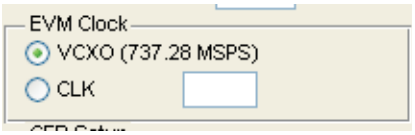
4.1.1 Step 1: Signal Setup

1. If the VCXO frequency is not the default 737.28 MHz, select the CLK option (as shown in the following inset) and input the clock rate in the text window.

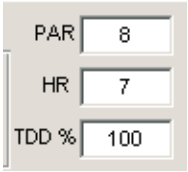


   In this example, a clock rate of 737.28 MSPS is used. ***The clock rate must be between 650 and 750 MHz.***

2. Input the complex sample rate of your input data if it is different than the default value. The input rate can be up to the EVM Clock rate divided by 12. For this example, the default value of 61.44 MHz (737.28 divided by 12) is used.

   The GC5325EVM GUI fractionally resamples the signal to match the GC5325 complex input rate of the EVM Clock divided by 12 (the interface uses an interleaved format for I and Q, so the actual data transfer rate is 2x).

3. Set the desired Peak to Average Ratio (PAR), Headroom (HR), and TDD% for the CFR block. Referring to the following diagram, Headroom is the clipping threshold relative to full-scale for the CFR block and PAR is the RMS level of the input signal below the Headroom. The GC5325EVM GUI rescales the input signal so as to set the RMS level appropriately. The TDD% value is used to compensate for the zero time of TDD downlink signals. If the downlink time is 60% of the frame, then the TDD% must be set to 60.



   For this example, the PAR and Headroom settings were kept as the default values of 8 dB and 7 dB. The PAR and HR settings can be adjusted later after the signal is loaded by selecting the PAR/HR button.

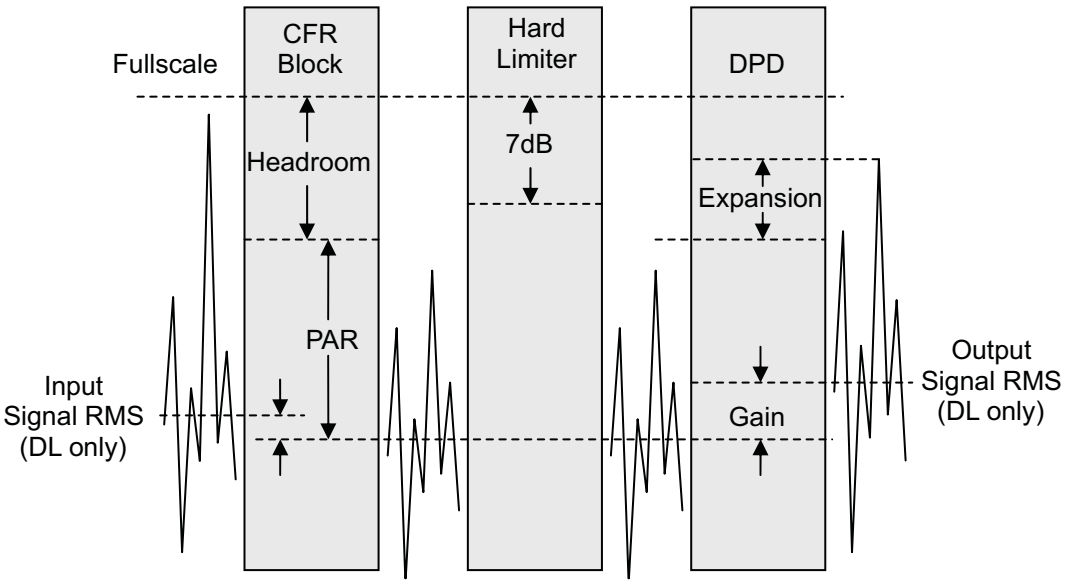


Figure 7. Signal Levels in the GC5325 – Definition of HR and PAR

Following the CFR block, a Hard Limiter block that limits the signal to – 7dB below full-scale. This is to ensure that the DPD block has 7 dB available for signal expansion and gain adjustment (compensating for analog gain variation).

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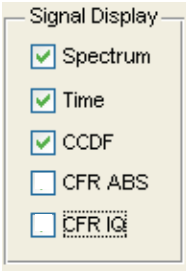
4. The Signal Display check boxes can be checked as needed to display the signal characteristics (Spectrum, ABS vs time, CCDF) of the input signal after resampling and gain adjustment. For this example, all the boxes are checked.



5. Now, the input signal can be loaded by clicking on the Load Signal button. The format of the input signal can be a complex MATLAB vector saved as a .mat file (Figure 8), or a two-column text file. Because the GC5325EVMGUI rescales the input signal to the appropriate RMS level, the input signal can be floating point and need not have any particular scaling. Browse to the appropriate file and select OK.

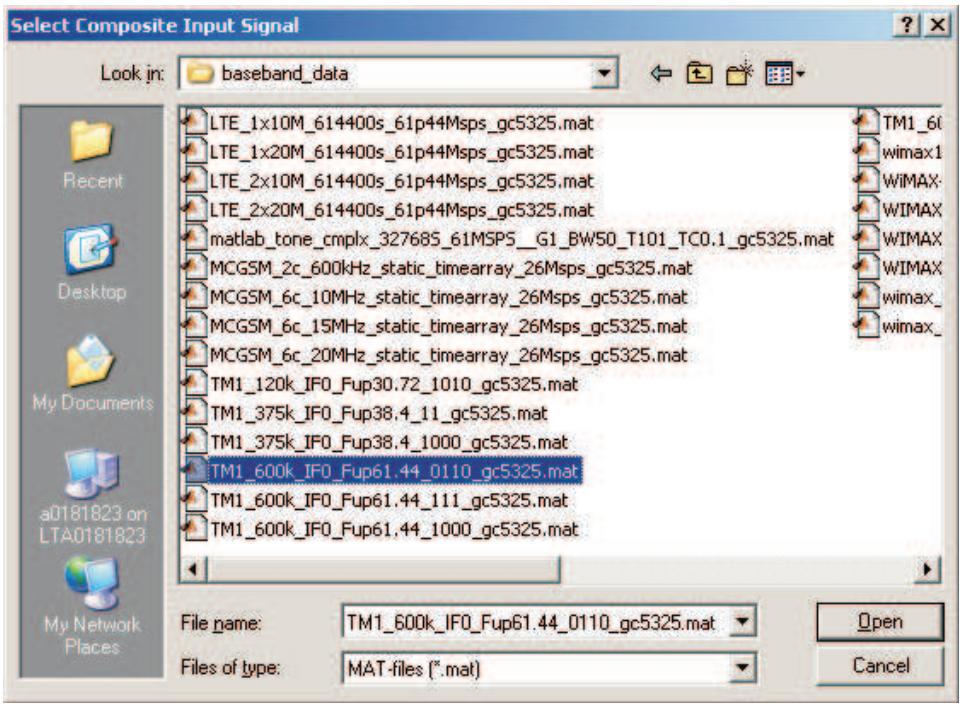


Figure 8. MATLAB Vector Saved as .mat File

Next, the Import Wizard properly delimits the input file and loads the signal. Click on Finish (Figure 9).

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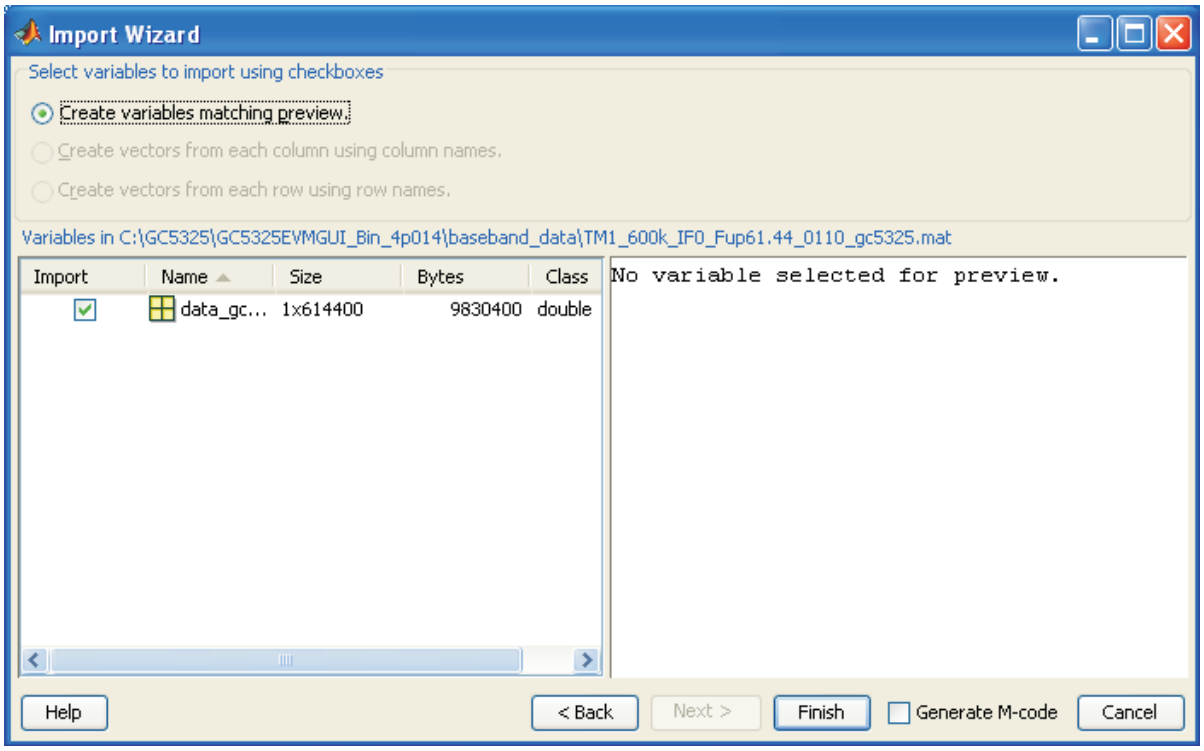

Figure 9. Import Wizard Screen

The Windows with the input signal characteristics pop up after loading. The first three are the Spectrum (Figure 10), ABS time series (Figure 11) and CCDF (Figure 12) of the resampled signal:

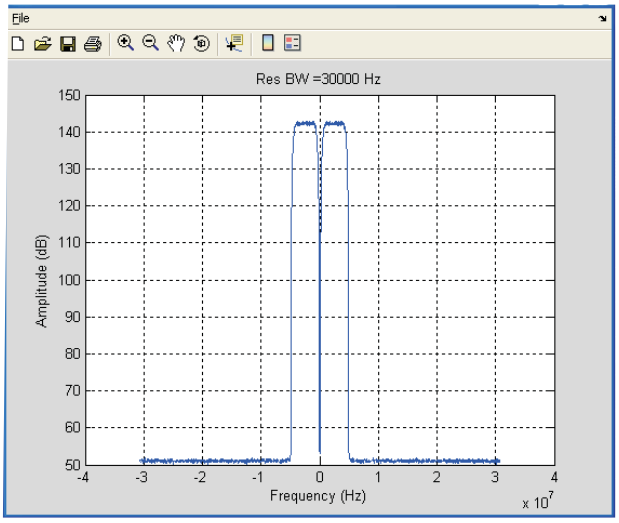

Figure 10. Spectrum

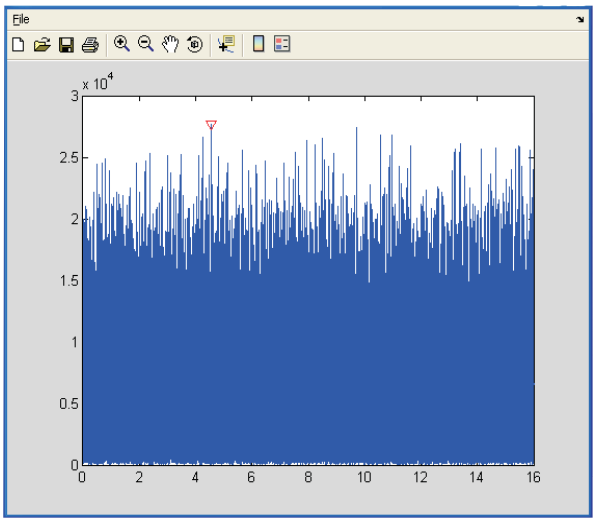

Figure 11. ABS Time Series

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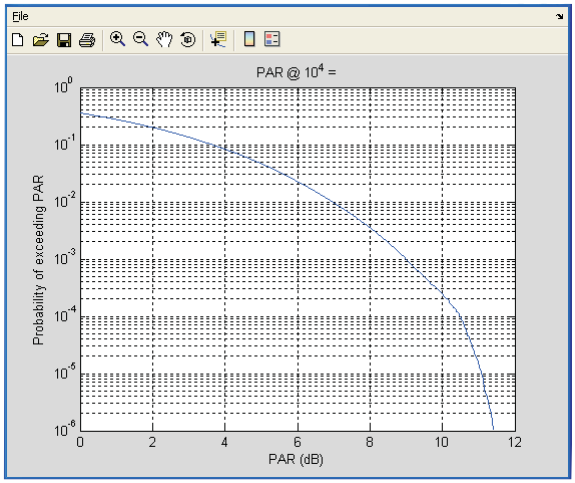

Figure 12. CCDF

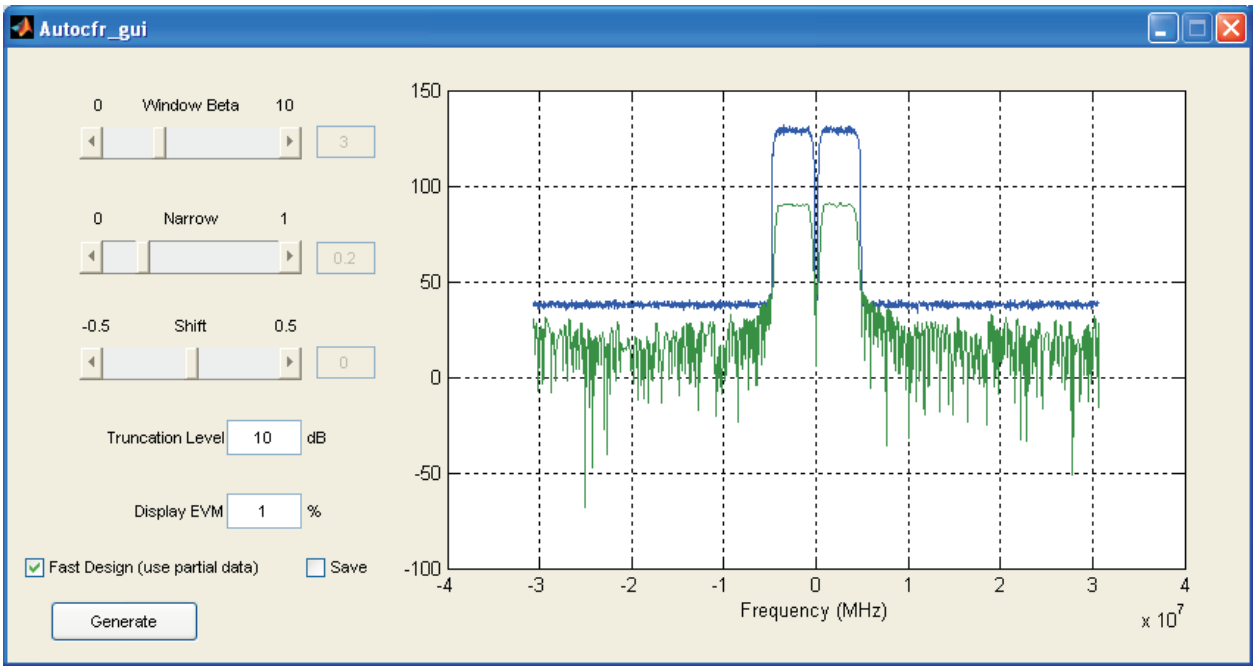

Figure 13. Autocfr_gui Window

The ABS time series plot also denotes the location of the sync A input signal (red upside down triangle) used by the GC5325 to capture data for DPD. A suitable time is found by the GC5325EVMGUI automatically and must be located in a region with active data (not during the zero time).

6. If the Auto Filter option in the CFR Setup were chosen, the Autocfr_gui window (Figure 13) opens:

The Autocfr_gui is a fast, simple method to design the CFR cancellation filter based on the spectrum of the input signal. The CFR filter has approximately the same spectral mask as the input signal, so that the noise energy generated by peak cancellation remains in band. The Autocfr_gui generates a CFR filter to match the input spectrum the first time it loads. If this looks acceptable, no other adjustments are necessary. Three main control values can adjust the spectral shape of the filter:

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- Window Beta (default = 3): The Autocfr_gui uses a window function for generating the CFR filter, and the amount of windowing is controlled by Window Beta. Increasing the Window Beta broadens the frequency of the in-band spectrum and lowers the floor of the out-of-band spectrum. Decreasing the Window Beta narrows the frequency of the in-band spectrum and raises the floor of the out-of-band spectrum.
- Narrow (default = 0.2): Increasing the Narrow value slightly narrows the in-band spectrum. This can be used to compensate for the broadening of the in-band spectrum due to increasing Window Beta.
- Shift (default = 0): The shift value shifts the in-band spectrum slightly to the left or right. Sometimes the CFR spectrum is slightly off from the input signal spectrum.

The four other controls for the Autocfr_gui are:

- Truncation Level (default = 10 dB): The truncation level defines the level from maximum spectral amplitude that is considered in-band. For example, if the input signal consists of three carriers with relative amplitudes of 0, –5 dB, and –15 dB, only the 0 and –5 dB carriers are considered in-band.
- Display EVM (default = 1%): This value only affects the relative amplitude of the CFR filter spectrum relative to the signal spectrum. This value must be set to the approximate in-band EVM target for CFR, and then adjusts the CFR filter spectrum relative to the signal spectrum in the display until the in-band amplitude difference is this value. Doing this allows examination of the out-of-band CFR noise relative to the spectral mask requirement. This does not affect any setting in the GC5325 or change the CFR filter – it only affects how the two curves are displayed on the graph.
- Fast Design: If checked, this speeds up the generation of the CFR filter by only using a section of the input signal. If unchecked, the entire input signal spectrum is used. It is recommended to first get the basic CFR filter spectral shape as desired, then uncheck Fast Design and regenerate. This removes some of the noise in the CFR filter spectrum.
- Save: If checked, this allows saving a two-column text file with the filter taps when the generate button is clicked.
- Generate: After adjusting the CFR filter parameters, click on the Generate button to store the filter in memory for loading to the GC5325.

4.1.2 Step 2: Loading of the GC5325EVM

The user must load both Channel 0 and Channel 1 configurations before attempting any testing of the system. To load Channel 0 of the EVM, including the DSP run time code, FPGA registers, the RF portion (DAC5682Zs, CDCM7005, attenuators, RF switches), GC5325 configuration, and TSW3100 Pattern Generator, click on the Load EVM button:

This results in a significant amount of information to be displayed in the programs DOS window. This takes approximately 60 seconds. When it is finished, the DAC5682Z "DLL locked" indicator is green on the GUI, indicating the DAC5682Z is locked to the GC5325. The Cal Feedback button in the DPD Control section is now enabled. The status message window in the bottom of the GUI now displays "EVM downloading is done."

Several indications on the GC5325EVM hardware show that the loading was successful. Near the DSP are four status LEDs, (Figure 14) which provide the following status:

1. The LED labeled DSP_CONFIG blinks, indicating that the DSP loading was successful.
2. The LED labeled GC_CONFIG illuminates, indicating that Channel 0 GC5325 device has been configured properly.
3. The LED labeled GC0_FAIL illuminates if Channel 0 GC5325 device did not configure properly.
4. The LED labeled GC1_FAIL illuminates if Channel 1 GC5325 device did not configure properly (check after Channel 1 is loaded).

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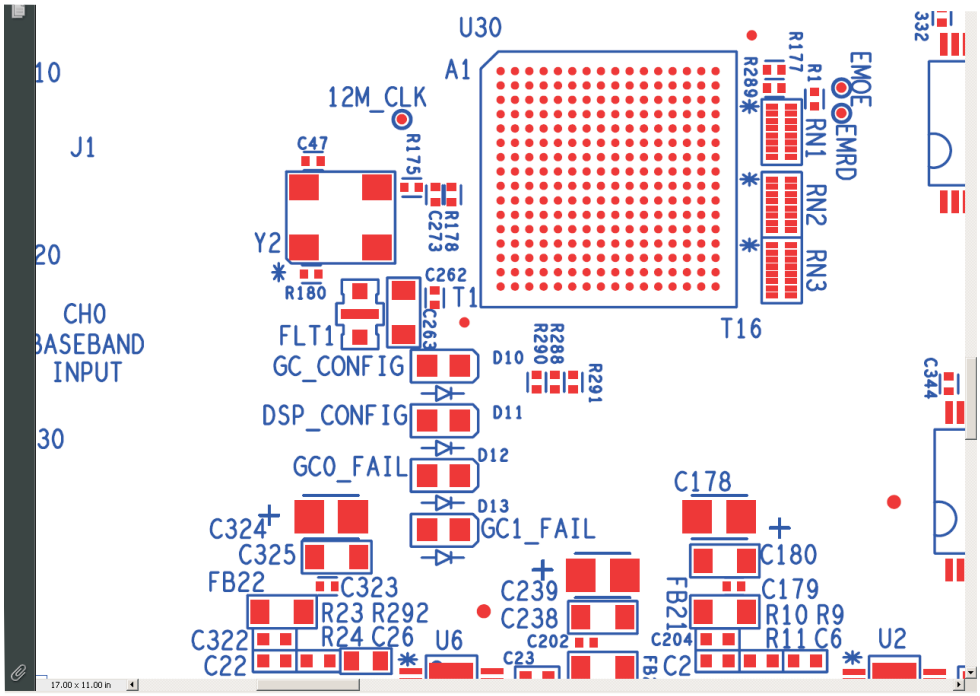

Figure 14. Status LED's

Near the middle bottom of the board, the three LEDs that indicate the status of the CDCM7005 (see Figure 15) should now all be illuminated.

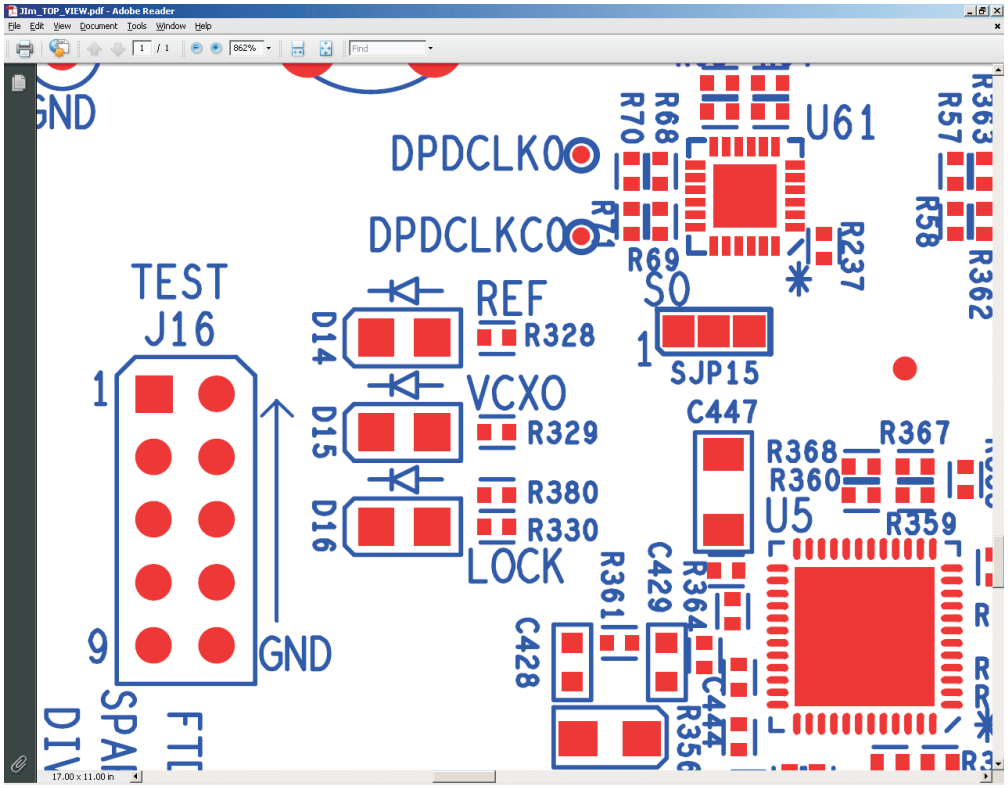

Figure 15. CDCM7005 Status LEDs

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The LEDs provide the following status:

1. D14 illuminates indicating that the 10-MHz reference clock is present.
2. D15 illuminates indicating that the VCXO is present.
3. D16 illuminates indicating that the VCXO is locked to the reference source.

If LED D16 does not turn on, there is a problem with the loading of the RF section of the board. Check the DOS window for any error messages. Verify the following if this situation occurs:

1. Make sure the dip switches are set properly.
2. Make sure the USB cable is installed between the USB-to-UHPI board and the host PC.
3. Make sure the DSP-Weuffen drivers are installed properly.
4. Make sure the USB-to-UHPI board is installed properly on the GC5325EVM.

When the TSW3100 pattern has been loaded properly into the TSW3100, the status LEDs of the TSW3100 change to indicate that the TSW3100 is now sending test data that was loaded to the GC5322EVM. The LEDs that are illuminated are shown in Figure 16.

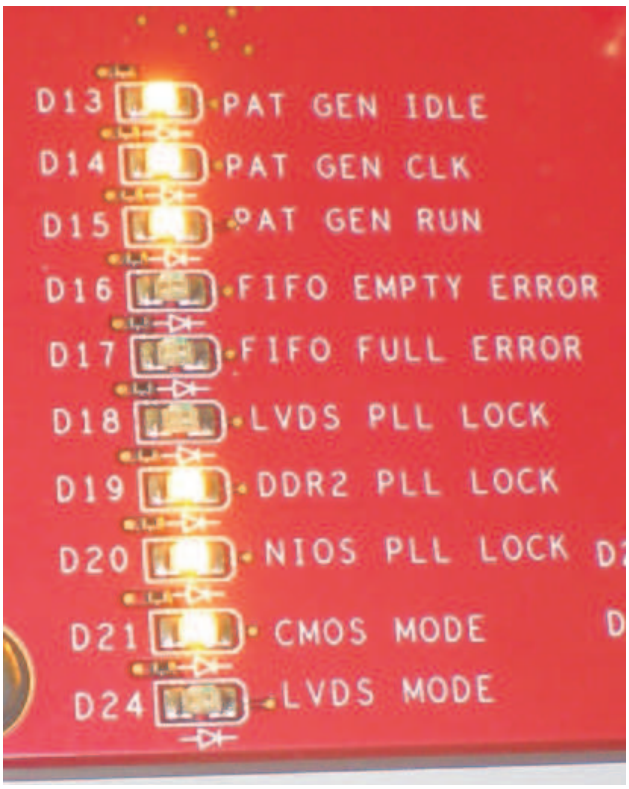

Figure 16. TSW3100 LED Status With Test Pattern Running

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NOTE: If these six LEDs are not illuminated after the TSW3100 has been loaded, make sure that the four power LEDs in the upper right side of the TSW3100EVM are illuminated. If any one of these are off, the board may have a possible power supply problem. If all four are on, a ping button located in the upper left corner of the GUI can be used to test the Ethernet connectivity. The IPdig is the last digit of TSW3100 IP address. It is 3 by default. To operate this test, click on the ping button. If the GUI is communicating with the TSW3100 properly, the following message appears in the DOS window as shown in Figure 17.

If the Ethernet connection is not working properly, make sure the two LEDs on the Ethernet connector on the TSW3100 are illuminated when the cable is plugged in between the board and the host with power applied to the board. If these LEDs are not on, try cycling the TSW3100 power and rebooting the host computer.

Other things to try are the following:

1. Disconnect the USB-Ethernet adapter cable from the host PC, then re-connect. Verify the USB connection is established.
2. Check that the Ethernet cable is plugged properly into the GC5325SEK and the LED's under the Ethernet connector are illuminated.
3. The USB-to-Ethernet adapter drivers are installed properly.
4. The Ethernet cable is a crossover cable
5. The dip switch on the TSW3100 is set properly.

NOTE: If there is an error with the data transfer across the USB-to-UHPI interface, an error message appears in the DOS window, and the GUI is disabled. If this occurs, the user must close the GUI, reset the DSP by pressing SW3 on the GC5325 EVM, and then re-open the GUI.

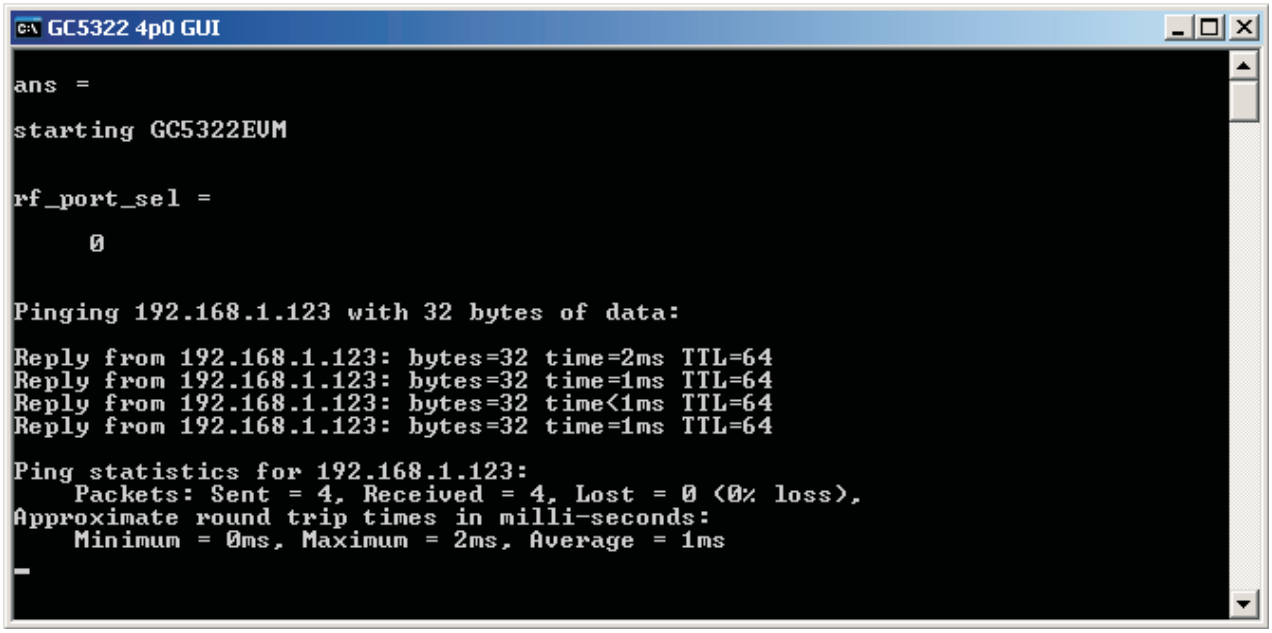

Figure 17. Ping Test Result

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4.1.3 Step 3: Loading Channel 1 Configuration Data

1. To load the TX Channel 1 devices of the GC5325EVM, including DAC5682Z, CDCM7005, attenuators, RF switches and GC5325, go to the "device button", located in the upper left side of the GUI, and change the current value from “0” to “1”. This now allows the GUI to communicate to the Channel 1 devices. To communicate with Channel 0 devices, simply switch this setting back to “0”.
2. Click on the “Load EVM” button:

   This results in a significant amount of information to be displayed in the programs DOS window and takes about 30 seconds. When it is finished, the “Cal Feedback” button in the DPD Control section is enabled and the GUI message window displays “EVM downloading is done” The DAC5682Z DLLlock indicator is green on the GUI reflecting the DAC5682z is locked to the GC5322.
3. Both channels are now configured and ready for test.

4.2 Operating the GC5325SEK

4.2.1 Controlling the Analog Signal and Running DPD

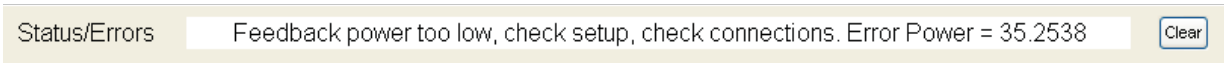
1. The test signals are now flowing through both GC5325 devices and the TX sections of the card. DPD has not started adaption at this point. The user first verifies the quality of the TX and FB path signals using the internal Capture Buffers in the GC5325s. For this test, the system uses the onboard loop back capability to loop the TX signal from Channel 0 back to the FB path. To enable this test, do the following:

   (a) Verify that the Loop back checkbox (located in the lower left section of the GC5325 GUI) is selected. If not, click on the box to select it. When Channel 0 loop back is enabled, LED D6 (next to SMA labeled TX0_OUT) is illuminated. When this is disabled, the channel is transmitting through this SMA and the LED is off. On power up, both channels come up in loop back mode to prevent from possibly overdriving external PAs. For Channel 1, LED D5 is illuminated when set to loop back mode.

   (b) The TX attenuator and RX attenuator settings can be adjusted in 0.25-dB increments by selecting the TX atten and RX atten boxes located in the bottom left side of the GUI. A value can be entered or the existing value changed by using the keyboard up and down arrows. The TX attenuator can be set from zero (minimum attenuation) to 31 (maximum attenuation) in 0.25 incremental values. For this example, set the TX atten to 5.

   Now click on “Cal Feedback” to set the RX attenuator for unity gain. Note that a complete path for the signal from DAC to ADC is required, either loopback or though external hardware. If successful, the RX Atten setting changes between 0 and 31. For the default internal loopback case, the RX attenuation typically is in the 5- to 15-dB range.

   If the power is not sufficient for the feedback ADC, you get the following error.



   An error has occurred where the feedback power is too high – in this case, attenuation must be added to the FB path input. If the Cal feedback is successful, the GUI status window displays the following message: "Calibration successful. RX attenuation set to XX," where XX is the setting programmed into the feedback attenuator. The Start DPD and Capture Buffer buttons now become active. Before Starting DPD, the user must examine the data from the capture buffers.

   Click on the “re-capture” button. This displays the DPD and Feedback output buffers on the GUI window, and now looks like the screen in Figure 18.

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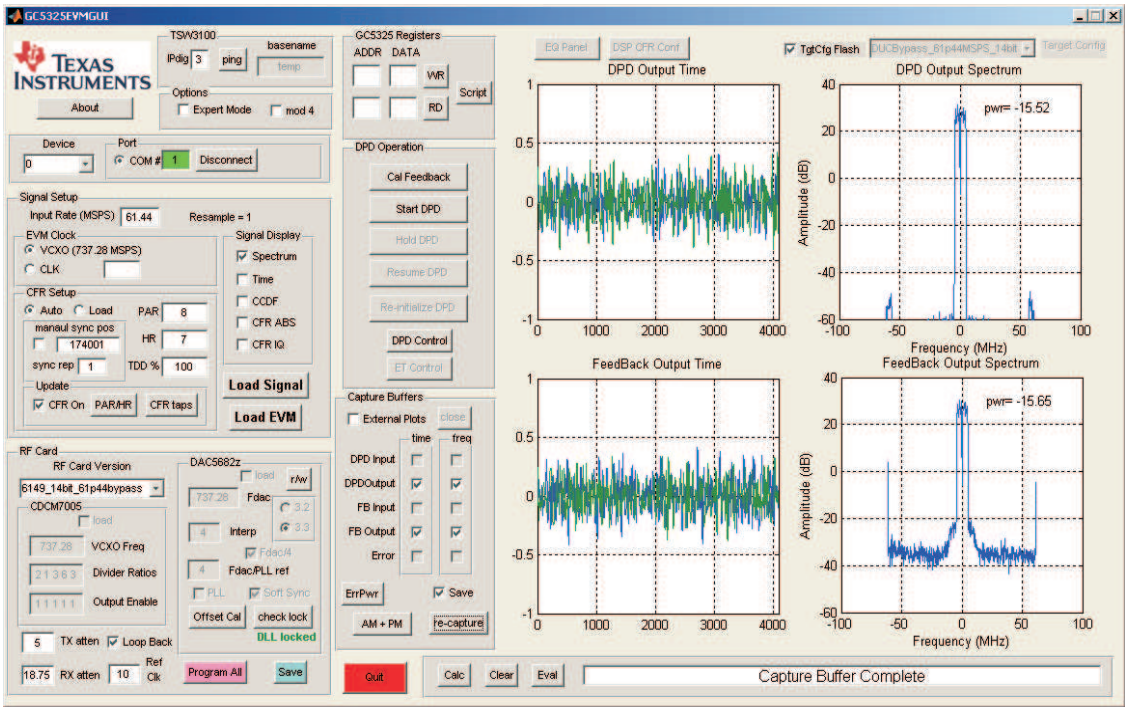

Figure 18. Loopback Results Using GC5325 Internal Capture Buffers

To view the DPD input, FB input, or Error capture buffers, the external plots check box needs to be checked. This opens the plots in separate windows. This is also useful if separate performance plots are needed for reports.

Both channels must be calibrated before starting DPD. Change the GUI device setting from "0" to "1" and repeat steps a-c. After Channel 1 has been calibrated, the user can now run DPD on Channel 0, Channel 1, or both at the same time. Change the GUI device setting from "1" to "0"

2. Start DPD by clicking on Start DPD. Once DPD starts, the system continues to adapt until the Hold DPD command is issued. All buttons except for Hold DPD and Re-initialize DPD are disabled.. To do any action such as capturing buffers, reloading the DSP/GC5322, etc., the user must click the Hold DPD button. If both channels are running DPD, both channels must be in the Hold DPD state to enable the other functional buttons.

   Click on the Hold DPD button. Click on the "re-capture" button. After the capture has been completed, the status window displays Capture Buffer Complete, and the GUI now looks as shown in Figure 19. The DPD output buffer and the Feedback buffer reflect the DPD operation on the internal loopback PA.

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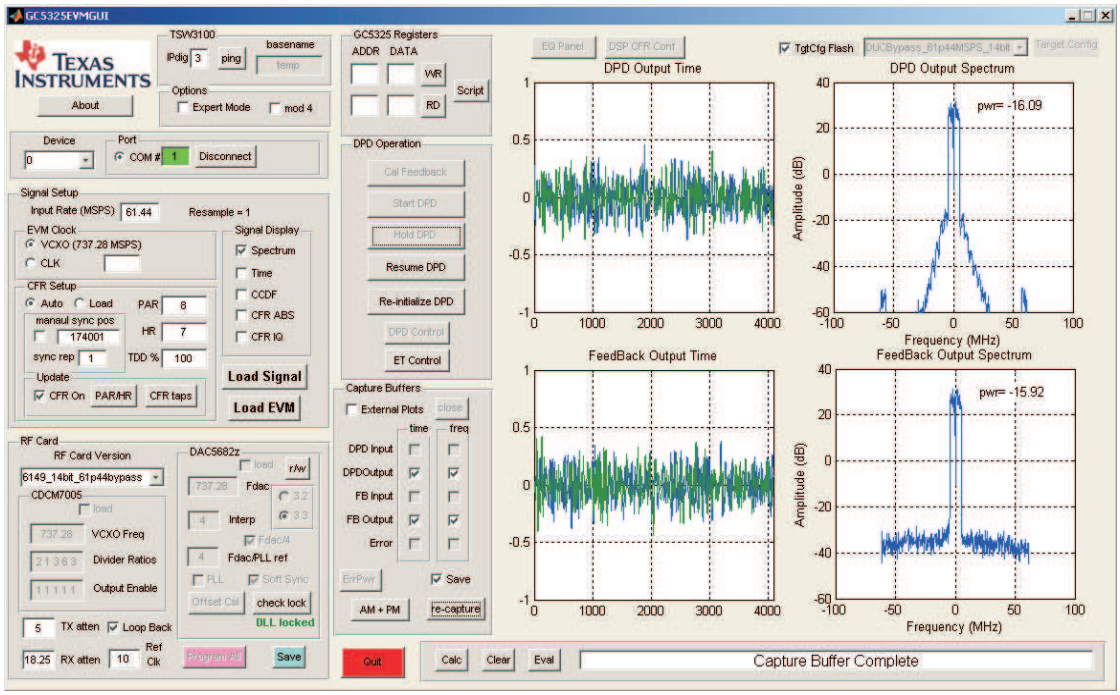
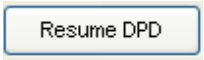


Figure 19. DPD Results From Internal PA for Channel 0

3. To resume adaption, click on Resume DPD.



The GUI then returns to the state where only Hold DPD and Re-initialize DPD buttons are active.

4. To restart DPD from the default loaded settings, click on the Re-initialize button. After clicking on Re-initialize, the user can adjust the CFR PAR and Headroom, CFR taps, TX Atten, Loopback, etc. If the TX atten setting is changed, a new Cal Feedback must be done.

4.2.2 Using External PAs

1. When operating with external PAs, the Loop Back mode must be disabled. When loop back is turned off for Channel 0, LED D6 turns off and LED D8 now turns on, indicating that Channel 0 is now transmitting across SMA connector J17 (TX0_OUT), and that the feedback path is now set up for RX0_IN. For this case, the feedback signal must be connected to SMA connector J46 (RX0_IN).
2. When using an external PA for Channel 1, disable Loop Back. LED D5 turns off and LED D7 now turns on, indicating that Channel 1 is now transmitting across SMA connector J18 (TX1_OUT), and that the feedback path is now set up for RX1_IN. For this case, the feedback signal must be connected to SMA connector J28 (RX1_IN).
3. When both channels are driving external PAs and running DPD, both LEDs D7 and D8 are blinking. When a channel is using the feedback path, the LED is on. Both lights blinking indicate that both channels are sharing the single feedback path.
4. After completing testing of the GC5325SEK, always shut down the GUI before removing power from the system. To close the GUI, click on the Quit button located at the bottom of the GUI, or click on the X in the upper right corner of the GUI window.

NOTE: If at any time during operation of the GC5325SEK GUI, the following error appears (as shown in Figure 20), just wait a second or two, then retry the last command that was attempted. In most cases, the DSP recovers and executes the next command. If a problem still exists, the DSP is probably locked, and the software must be closed, and reset the hardware by either pressing the DSP reset switch or cycling the power.

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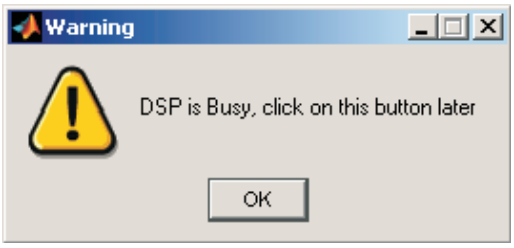

Figure 20. DSP Busy Warning

5 Other Functions

5.1 About

Clicking on "About" opens a widow that will display the GUI version.

5.2 TSW3100

The IPdig window displays the last address byte of the Ethernet address assigned to the TSW3100 EVM. The host PC will use this information to communicate with the TSW3100. Click on the Ping button to do a ping test between the host and the TSW3100. The complete default address is 192.168.1.123. If the last byte of the TSW3100 Ethernet address is different than this, the value will have to be entered into this window. Basename is not used

5.3 Options

Clicking on the “Expert Mode” button allows the user to do the following functions:

TX EQ plot - Displays the TX equalizer response using default unity. Click on the "EQ Panel" (see Figure 21) button to open a new window. Then click on the "TXEQ Plot" button to generate the plot. To invert the feedback signal spectrum, click on the "invert_eq_fb_flag" box. After doing this, the user must re-initialize DPD.

DSP CFR Conf - Allows the user to use predefined CFR prototype filters as opposed to using the auto composite filter generated by the GUI. This is explained in more detail in section 5.7.

Target Config - This window Indicates which target configuration (TGTCFG) file will be loaded into the GC5325. This window allows the user to load one of two predefined TGTCFG files (11bit or 14bit version) or custom version by selecting one of the files from the pulldown arrow on the Target Config window This window is only active if the expert mode is selected and the TgtCfg Flash box is deselected.

TgtCfg Flash box - Do not use.

mod 4 - Do not use.

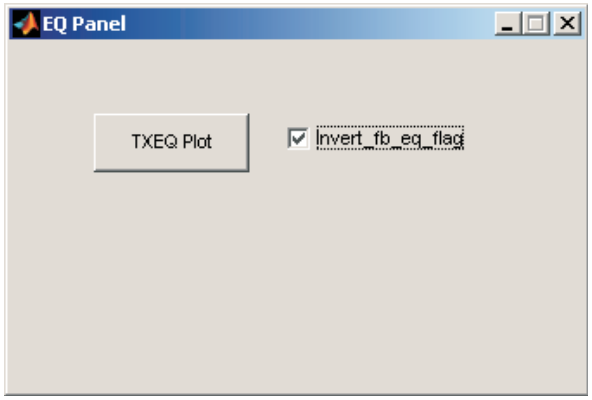

Figure 21. TXEQ Panel

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5.4 Device

Selects the TX channel (0 or 1) devices that the GUI is communicating with on the GC5325 EVM. This includes the GC5325, DAC5682Z, and attenuator.

5.5 Port

Do not use.

5.6 GC5325 Registers

The GC5325 Registers window (see Figure 22) allows the user to manually write and read the GC5325 internal registers. To write to a specific register, input the address and data in hexadecimal representation in the top boxes in the Registers box, and then click the WR button.

To manually read the GC5325 registers, input the address in hexadecimal representation in the bottom-left box in the Registers box, and click the RD button. The read value is then displayed in the Data box.

Another option is to uses scripts. Clicking on the "Script" button brings up a file browser to let you open a script file to run. The first character of the script file must be e or E, followed by white space, then the string to evaluate. No quote marks are needed. You can do multiple commands, but only on one line. The following example will open two figures and displays the number "1" followed by "2".

The content of myScriptExample.txt:

e for index = 1:2 figure(index); disp(num2str(index)); end

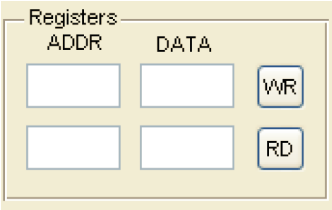

Figure 22. GC5325 Register Window

5.7 Signal Setup.

Input rate (MSPS) - This is the data rate of the baseband signal. The GUI will resample the data to align with the VCXO that is currently used on the EVM.

EVM Clock - This section specifies which clock source to use. The on-board VCXO is 737.28 MSPS. If this source is bypassed to use an external source, the user needs to select the CLK option and enter the frequency to be used.

Signal Display - This is used to display various plots of the input signal.

CFR Setup - The *Auto* option generates a filter based on the composite input signal. The *Load* option is used to load in a predefined CFR filter.

This filter would be loaded during the process of loading the input test signal. To load a custom CFR filter, select the *Load* option in the CFR setup section of the main GUI, as shown in Figure 23.

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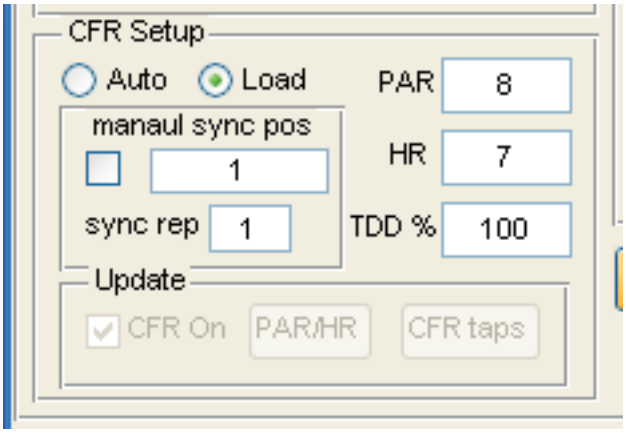

Figure 23. CFR Setup Window

Click the "LOAD SIGNAL" button then choose the composite input signal to be used. Once the input signal has been imported by the Signal Wizard pop up, the GUI will require the user to import data to be used as the CFR taps file, as shown in Figure 24.

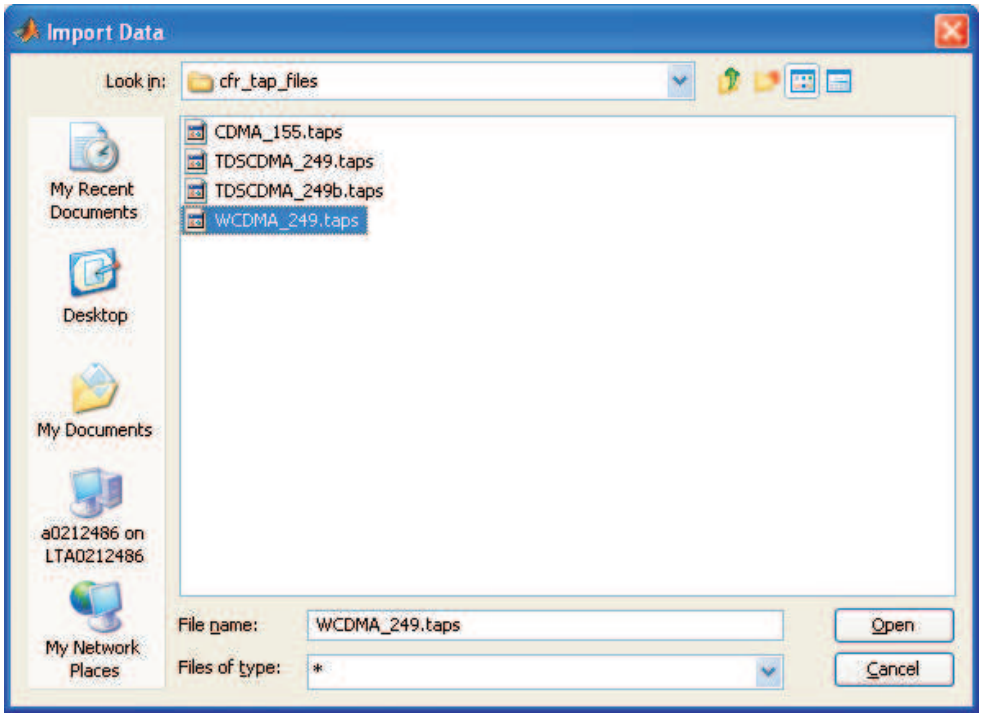

Figure 24. CFR Tap files directory

The GC5325SEK software contains four such files under the C:\GC5325GUI\cfr_tap_files directory. Choose a custom .taps file to be loaded for the CFR coefficients. When the Import Wizard opens, click on "Next", then "Finish".

PAR - This box specifies the desired output PAR.

HR - This box is the digital backoff reserved for DPD expansion. This is normally 7dB.

TDD% - This is the percent ON of the TDD input baseband signal. This must be specified before loading the test signal.

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manual sync pos - This is used to manually set the start of the initial capture buffer. Normally this position is calculated automatically by the GUI.

sync rep - Specifies the number of syncs. Typically, only one sync is required.

Update - Selecting CFR ON turns on the CFR block. The PAR/HR button is used to update the signal after changing the PAR and or HR settings. The CFR Taps button is used to update the CFR coefficients.

DSP CFR Conf - This button, located at the top middle of the GUI, is used to open a pop up (see Figure 25) to allow the user to specify a carrier configuration which the DSP will use to calculate the CFR filter coefficients based on carrier prototype filters. To enable the DSP CFR CONF button, the user must first click on the Expert Mode option. This is different from the wideband composite CFR filter generation done in the Auto CFR calculation on the host computer.

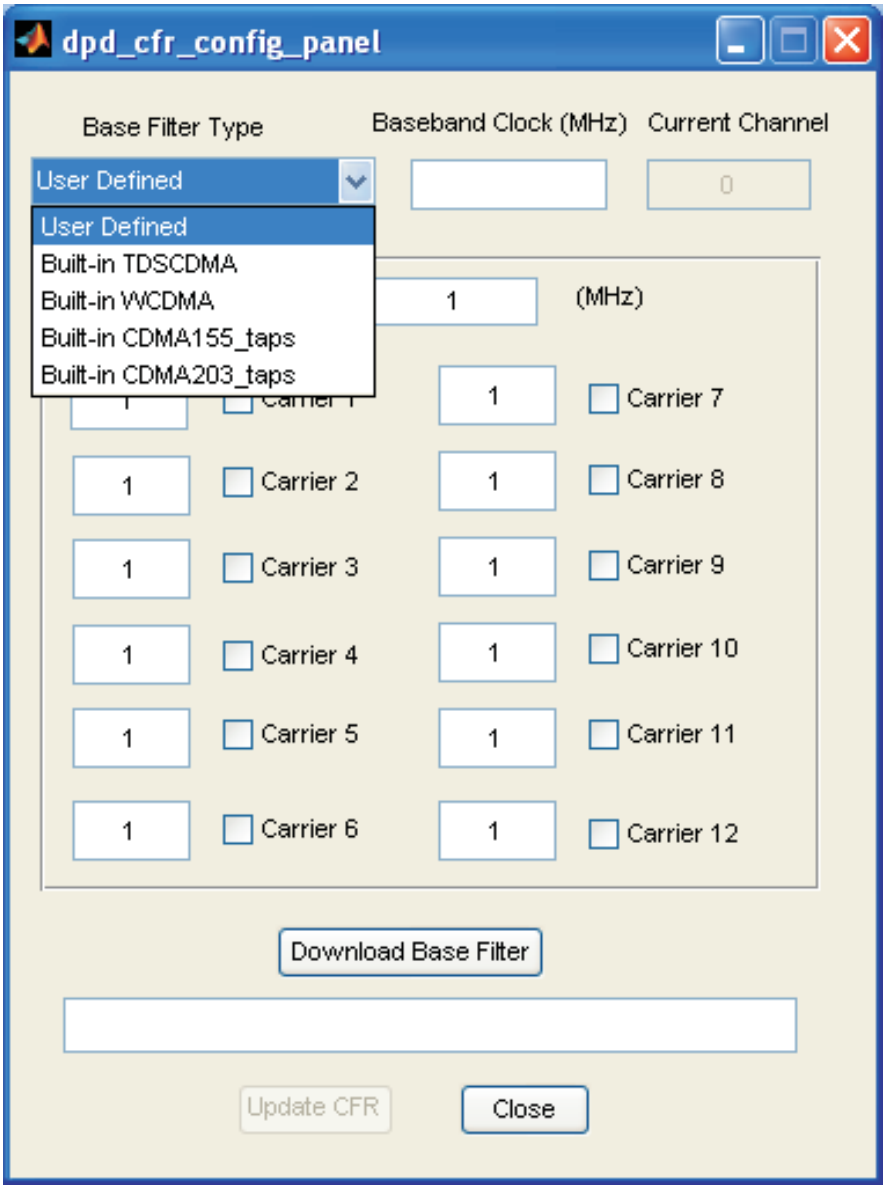

Figure 25. DPD CFR Configuration Window

The type of signal, baseband sampling and carrier location is specified and then sent to the DSP to calculate and update the CFR coefficients.

Load Signal - This button loads the composite input signal into the GUI for processing. This will cause the signal to be rescaled if needed based on the VCXO and sample rate

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Load EVM - This button programs the CDC clock generator, loads the test pattern into the TSW3100, loads the TgtCfg file, progams the DAC, and programs the TX and RX attenuators. This needs to be done for both CH0 and CH1

5.8 RF Card

RF Card Version - This button selects a predetermined file which contains the information that will be loaded into the programmable devices in the RF section of the GC5325 EVM. The default value, “6149_14bit_61p44bypass”, is used for the 14 bit ADC feedback version of EVM. The 11 bit option is used for China configurations which is different due to export control limitations. The differences are the sample rate and signal IF. A “custom” option can be selected, which allows the user to set custom values for the CDCM7005 outputs. The user should not change the default setting.

Load – Used to load a custom configuration for the CDCM7005. Typically, this is not used.

VCXO Freq – Specifies the VCXO frequency to be used by the CDCM7005. The on-board VCXO is 737.28 MHz. If an external VCXO is to be used, the value needs to be entered here.

Divider Ratios - This is the divide value used by each of the CDCM7005 outputs. The first number is the divide ratio for the FPGA clock, the second the DAC clocks, the third GC5325 DPD clocks, the fourth is connector J49, and the last the ADC clock.

Output Enable - This is the enable value used by each of the CDCM7005 outputs. The clock is enabled when this is set to a “1”, and disabled when set to “0”. The assignment order is the same as the Divider ratios.

TX atten - This box is used to set the attenuation value of the TX attenuator. The range is from 0 to 31.75, using increments of 0.25, with 0 being minimum attenuation and 31.75 the maximum attenuation.

RX atten - This box is used to set the attenuation value of the RX attenuator. The range is from 0 to 31.75, using increments of 0.25, with 0 being minimum attenuation and 31.75 the maximum attenuation.

Loop back - This button is used for internal loop back testing using an on-board amplifier. When this is selected, the transmit data is removed from the output SMA and re-routed to an amplifier which then feeds this signal into the receive path. The external receive signal from the SMA is removed from this path as well in this mode. The board will power up in this mode by default.

Ref Clk - This window is the frequency (in MHz) of the on-board reference oscillator.

DAC5682z - This section allows the user to change certain settings of the DAC5682z devices. The “r/w” button allows the user to write and read from the internal registers of the DAC’s. FDAC is the frequency of the DAC clock. Interp is the interpolation setting of the DAC.

load - Used to load a custom configuration for the DAC5682Z. Typically, this is not used.

Fdac/PLL ref - Used for custom DAC PLL setting. Typically, this is not used.

PLL - Selects PLL mode or external clock for DAC's.

Soft Sync - Used to select the sync method for the DAC's.

Check lock - This button checks the status of the DAC DLL.

Offset Cal - Clicking on this button will open a new window as shown in Figure 26. This window is used to null the LO feedthrough at RF by using the DAC5682Z offset capability. To do this, monitor the power of the LO feedthrough at RF, select OFFSET CAL, and adjust until the LO feedthrough is minimized.

Program All - This button will load the Rf devices with the current settings inside the RF Card section.

Save - Will save the settings inside the RF Card section to a user determined file.

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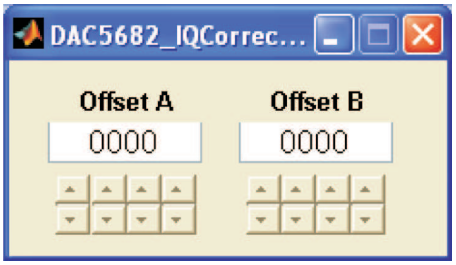

Figure 26. DAC5682Z Offset Correction Window

5.9 DPD Operation

The DPD Operation section contains the following modes of operation:

Cal Feedback - This button, when selected, will start calibrating the RX attenuation to normalize the feedback gain.

Start DPD - This button, when selected, will start the DPD adaptation. This button will only become active after a successful calibration feedback has been performed.

Hold DPD - This button will hold the Look Up Tables (LUT) and stop DPD adaptation.

Resume DPD - This button will resume adaptation after a Hold DPD was issued.

Re-Initialize DPD - This button resets the adaptation.

DPD Control - This button can be used when the DPD is initialized to change the Polynomial order for the algorithm. The 4 values correspond to the highest order polynomial used for the PA Model, Z = -1, 0, and +1 Look Up Tables (LUTs). Z = 0 LUT is the memoryless predistortion, while Z= -1 and +1 are correspond to the memory effects. The default setting is 15 for each, although typically only a value of 9 or less is needed. Lowering the value will speed up the adaption time of the algorithm.

In most cases, the Model and Z = 0 values should be the same and the Z = -1 and +1 values should be the same. Often the Z = -1 and +1 values can be less than the Z = 0 value.

To enable DPD Long, click on the "DPD Long Enable" button. Set the desired number of Taps (between 1-10). After the changes have been made, click on the "Update" button. After any changes to either Short or Long DPD Adaptation, the user must re-initialize DPD.

To write and read from the DSP memory, simply enter the address/data in the correct boxes and then click on either the "Read" or "Write" button. Consult the GC5325_DPD_Software_User's_Guide for valid DSP memory locations that can be accessed with this tool.

To set the value in the DSP algorithm, click on the "DPD Control" button, located inside the DPD Operation window. The DPD Control widow will open as shown in Figure 27. Use the pull down menus to set the values and click on the *Set* button

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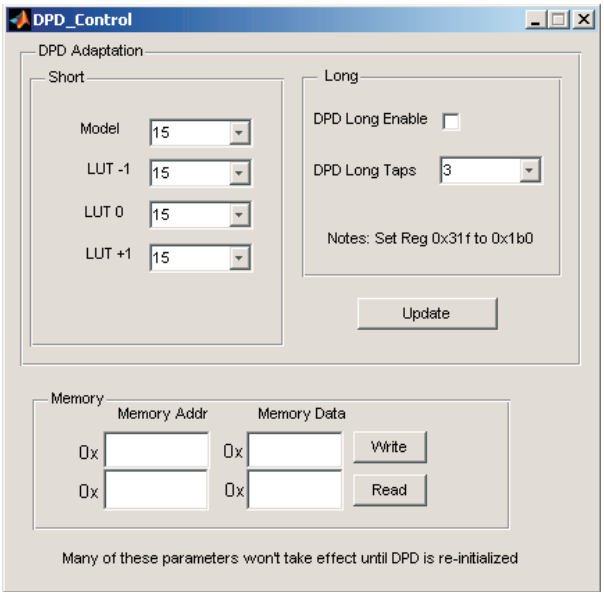

Figure 27. DPD Control Window

ET Control - Will be addressed in a future application note.

5.10 Capture Buffers

The Capture Buffers window allows the user to capture 4K of data from different points of processing within the GC5325. The GC5325 contains two 4K capture buffers which will store the data that is selected by the user. The Capture Buffers are the 4 plots located on the right side of the GUI. The top two displays (time and frequency) use data from one capture buffer and the bottom two displays use data from the other buffer. The top two displays show the DPD output data. This is the pre-distorted signal data from the transmit buffer. The bottom two displays show the feedback output data. This is the feedback buffer complex data that is converted to baseband. The following can be viewed when they are selected and the "External Plots" box is selected:

Selecting "DPD Input" displays the data captured by the input buffer which feeds the DPD algorithm.

Selecting "FB Input" displays the input buffer at the feedback (ADC).

Selecting "Error" displays the Feedback signal compared to the original TX signal from the TSW3100.

External plots allows external plots to be plotted and saved.

ErrPwr - This button displays the error power between the TX and RX buffers.

AM + PM - This button makes either a PA AM-AM (amplitude vs amplitude) plot, as shown in Figure 28, or a AM-PM plot (amplitude vs phase). The blue curve was taken before DPD. The green and red ones were taken after DPD. The plot will hold the previous plots and overlay any new plots that are taken. To clear existing plots, close the plot and start over.

The AM-AM plot shows the normalized amplitude variation at the PA output over the range of the signal amplitudes at the PA input. The X axis is the range of the input amplitudes, and the Y axis is the variation in amplitude at the PA output. This gives an indication of the amplitude response of the PA at a particular operating point. For a PA that is linear, the amplitude variations would be close to 0 dB across all input amplitude ranges since the normalized PA output tracks the PA input. As the PA starts to operate near saturation, the PA output response may show both compression and expansion effects which is reflected in the AM-AM plot. The larger amplitude variations at the smaller signal levels are mainly due to normalization of small errors to even smaller signal amplitudes.

The AM-PM plot is similar to the AM-AM plot. However, the AM-PM plot shows the phase variation of the output signal relative to the phase of the input signal over the range of input signal levels.

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This plot shows the phase response of the PA at a particular operating point. When the PA is operating in a linear region, the phase response are linear and shows near 0 degrees of variation. As the PA operates near saturation, the phase difference will change.

In both cases, the AM-AM and AM-PM plots are useful to help understand the PA amplitude and phase response before and after linearization.

Re-capture - Clicking on this button displays the settings selected in the Capture Buffer section.

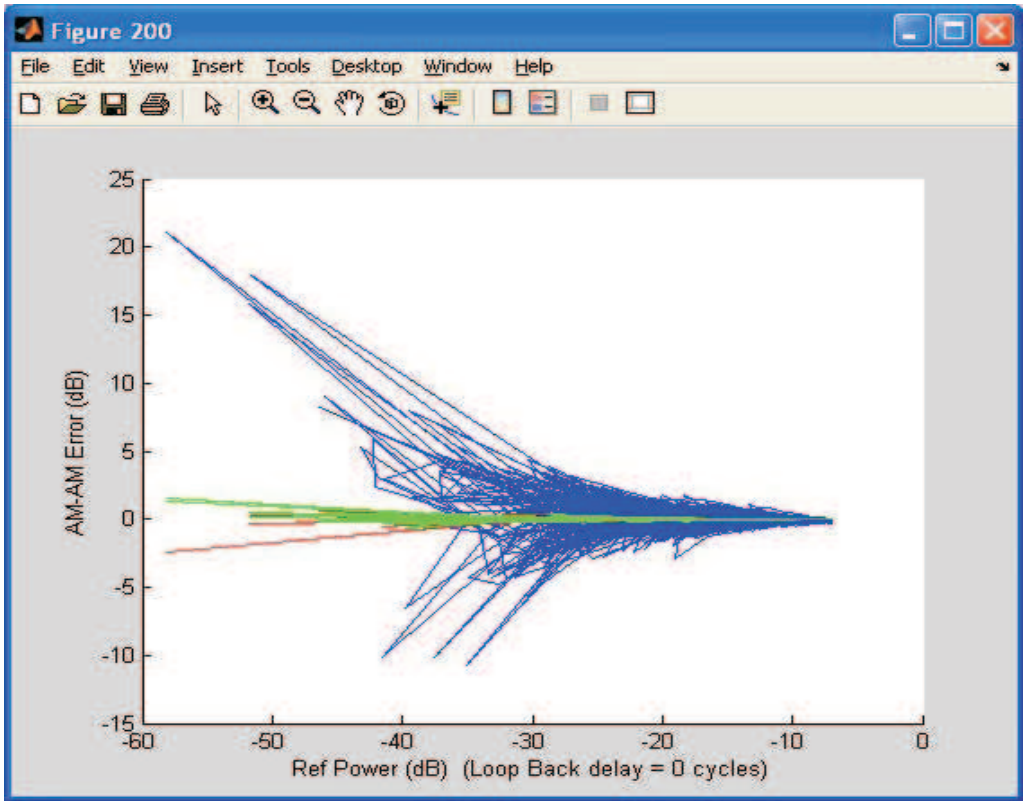

Figure 28.

5.11 Quit and Command/Message window

Quit - To quit the GUI, click on the “QUIT” button located at the bottom center of the GUI. This should always be done before powering down the EVM.

Calc - This button opens a windows calculator when selected.

The command/message window displays the command that the DSP and SPI bus is currently processing. Commands can also be issued by entering the appropriate text in this widow and clicking on the Eval button. This feature is not recommend to be used. The “Clear” button clears the command/message window. The “Eval” button will evaluate the command entered in the command/message window. This is used internally for debug reasons.

6 Summary

If the user has successfully completed the preceding steps, the system has applied linearization to one or two PAs at a user-defined power level. Additional power amplifiers can be tested over various operating conditions using the appropriate steps previously outlined. Additional functions may be required, and the users are encouraged to request these from Texas Instruments through their local support group. This guide does not support custom DUC, CFR, or DPD settings, although this is possible.

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Appendix A LEDs, Switches, Connectors, and Jumpers

A.1 TSW3100 LED, Switches, and Connectors

Power and status LEDs on after power is applied:

D3 – 2.5 V present
D4 – 1.8 V present
D5– 1.2 V present
D6 – 3.3 V present
D11 – FPGA configured
D13 – Pattern Generator Idle
D19 – DDR2 PLL Lock
D20 – NIOS PLL Lock

D23 – +1.8 Vdc and +3.3 Vdc external power supply ON

Status LEDs ON after pattern is loaded successfully

D13 – Pattern Generator Idle
D14 – Pattern Generator CLK present
D15 – Pattern Generator Running

D16 – FIFO Empty Error
D17 – FIFO Full Error
D18 – LVDS PLL Lock

D19 – DDR2 PLL Lock
D20 – NIOS PLL Lock
D21 – CMOS Mode
D24 – LVDS Mode

Table 1. TSW3100 Jumper and Switch Description

Designator	Description	Default Position
J50	Clock select. 2-3 for onboard oscillator. 1-2 for SMA J41	2-3
SW2	Sets Ethernet address and invert option for CMOS output clock. See TSW3100 User's Guide for more information	All set to "Open"
SW1	Board main power switch	"ON"
SW5	External 1.8-Vdc and 3.3-VDC output supply. Not used with the GC5325SEK	"OFF"
S9	FPGA Config. Press to reload FPGA configuration prom code into the FPGA	
S8	Spare	Not Used
S7	Start/Stop. Used to stop and re-start pattern generator. See TSW3100 User's Guide for more information	
S3	Sync. Sends a one-time Sync pulse at the start of the test pattern	

Table 2. TSW3100 Connectors

Designator	Description	Default Position
J63	Baseband connector for GC5325	Connect to GC5325 EVM J1
J64	Baseband connector for GC5325	Connect to GC5325 EVM J3
J73	CMOS baseband CLK input from GC5325	Connect to GC5325 SMA J2
J13	Ethernet connection to PC for pattern load	Connect to Host PC via USB-Ethernet adapter
J9	Power input connector from GC5325	Connect to GC5325 J22

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A.2 GC5325EVM LED, Switches, and Connectors

Status LEDs after power is applied:

D1-D4 – FPGA firmware revision
D7 – On when Channel TX0 is transmitting at output connector.
D8 – On when Channel TX1 is transmitting at output connector.
D5 – On when Channel TX1 is in Loop Back Mode.
D6 – On when Channel TX0 is in Loop Back Mode.
D9 – FPGA Configuration Complete
D10 – On after both GC5325 devices are configured.
D11 – Blinking after DSP is up and running.
D12 – On (Red) when GC5325 device 0 fails to configure properly.
D13 – On (Red) when GC5325 device 1 fails to configure properly.
D14 – On when CDCM7705 reference source is present.
D15 – On when CDCM7005 VCXO source is present.
D16 – On when CDCM7005 outputs are locked to the reference.
D17 – On (Red) when RS-232 interface is not connected or transmitting data properly.
D18 – Not used
D19 – Not used
D20 – On (Red) when the ADS61B49 input is out of range.

Table 3. GC5325EVM Jumper and Descriptions

Designator	Description	Default Position
NC – NOT CONNECTED		
SJP16	CDC VCXOP select. Set to pins 2-3 for internal VCXO operation, pins 1-2 for external VCXO operation.	2-3
SJP17	CDC VCXON select. Set to pins 1-2 for internal VCXO operation, remove for external VCXO operation	1-2
SJP14 SJP15	GC5325 clock buffer control GC5325 clock buffer control	2-3 2-3
JP1	10MHz REF POWER. Set to pins 2-3 when using external reference source.	1-2
JP2	10MHz REF CLK SEL. Set to pins 2-3 when using external reference source.	1-2
SJP5 SJP6	Not used	1-2 1-2
SJP8	RX_LO Select. Set to pins 1-2 to use TX_LO source. Set to pins 2-3 for RX_LO source from SMA J19	1-2
JP9	FB Mixer PWR/GND select. Active mixers use PWR, passive mixer use GND	1-2
JP6	FB Mixer PWR/GND select. Active mixers use PWR, passive mixer use GND	1-2
SJP12	INT/EXT FB Mixer output select. Set to pins 1-2 for internal Mixer, 2-3 for external	1-2
JP7	Mixer select Control 1	2-3
JP8	Mixer select Control 2	1-2
SJP11	INT/EXT FB Mixer input select. Set to pins 1-2 for internal Mixer, 2-3 for external	1-2
JP10	CDCM7005 VCXO Power.	installed
SJP9	IF filter output select.	1-3
SJP10	IF Mixer output select	1-3
SJP7	EEPROM Write protect	2-3
SJP13	INT/EXT mixer LO select	1-2
JP5	FLASH device write protect	1-2
SJP1	GTRST for JTAG chain	1-2
SJP2	DSP_DO for JTAG chain	1-2
SJP3	FDO for JTAG chain	2-3
SJP4	JT_OE for JTAG chain	1-2
SJP19	5V for external UHPI interface connector	1-2
SJP18	3.3V for external UHPI interface connector	OPEN

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Table 3. GC5325EVM Jumper and Descriptions (continued)

Designator	Description	Default Position
SW1	SPARE	
SW2	Hardware Reset	
SW3	DSP Reset	
SW4	Main board power switch	
SW5, SW7	DIP switches used to control operation of FPGA and DSP.	See section 2, on page 6
SW9	Re-load FPGA configuration file	

Table 4. GC5325EVM Connector Description

Designator	Description
J30	External VCXO input if the internal VCXO is bypassed with resistor options
J35	Spare CDCM7005 CMOS output clock
J33	External Reference for CDCM7005 if internal 10M is not used
J34	10MHz reference clock output to drive external test equipment
J37, J38	RF signal test connector at modulator outputs
J44 J4	CH 0 TX modulator LO test connector CH 1 TX modulator LO test connector
J32	CH0 TX output test connector after amplifier and attenuator.
J17	CH0 TX Output
J29	CH0 loopback test connector
J46	TX0 feedback input connector (RX0_IN)
J19	Optional RX_LO input connector
J2	PG_CLK_OUT used to provide master clock to the TSW3100
J18	CH1 TX Output
J36	CH1 TX output test connector after amplifier and attenuator.
J39	CH1 loopback test connector
J28	TX1 feedback input connector (RX1_IN)
J21	FB RF test connector
J9	External Filter_Out
J6	External Filter_In
J10	External LO_IN
J13	External +5V_IN
J41	RF signal test point for LO signal before RX feedback mixer
J42	RF signal test point for RF feedback signal just before mixer
J43	RF signal test point for IF feedback signal at mixer output
J5	RF signal test point for injection of signal into IF filter – for characterization purposes
J40	IF signal test point, monitor IF frequency response of IF filter/RX signal chain
J23	Optional Main power input connector
J11	FPGA JTAG connector
J20	Main LO input. Used for both TX and RX devices (default setting)
J14, J15	BYPASS - EXTERNAL FILTER IN AND FILTER OUT
J7	19V input power connector
J12	EXT_FPGA_CLK
J16	FPGA test connector
J25, J26	External UHPI interface connectors
J27	DSP JTAG connector
J31	RS-232 connector
J1, J2	Baseband input from TSW3100

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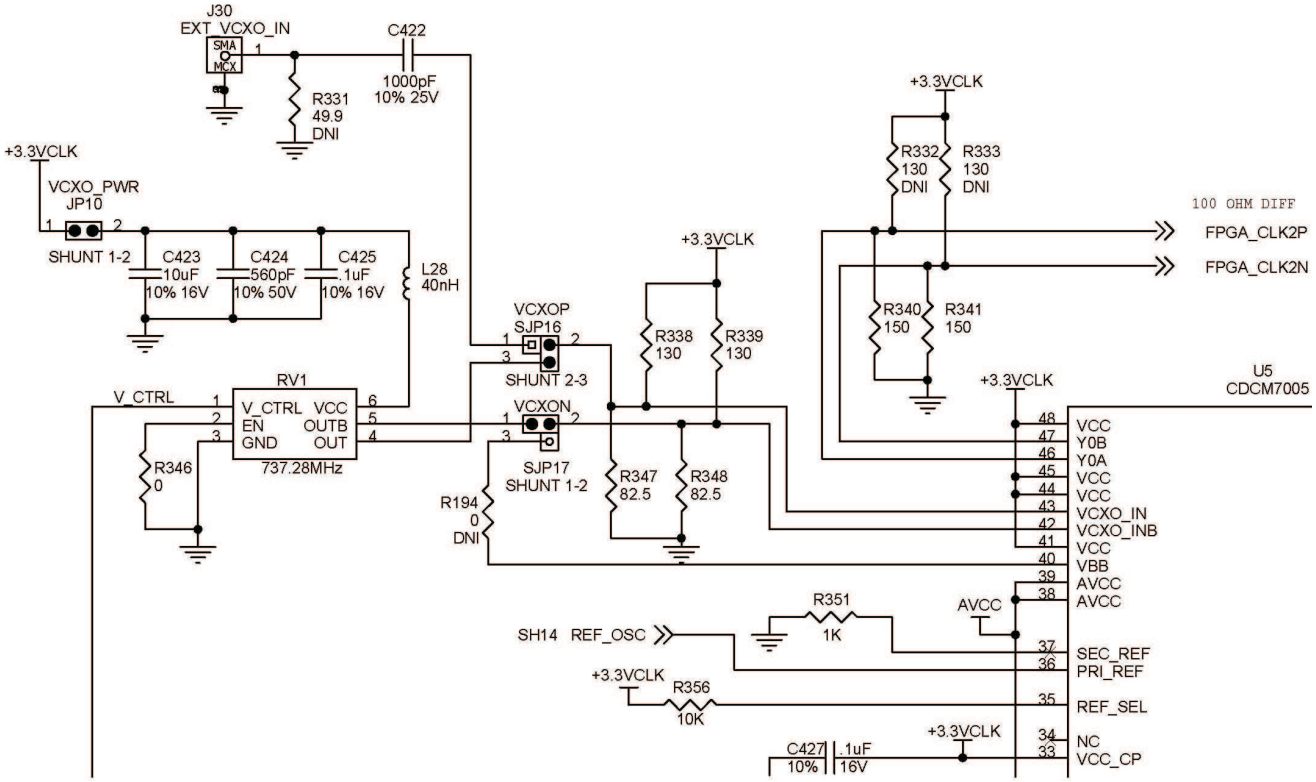
Table 4. GC5325EVM Connector Description (continued)

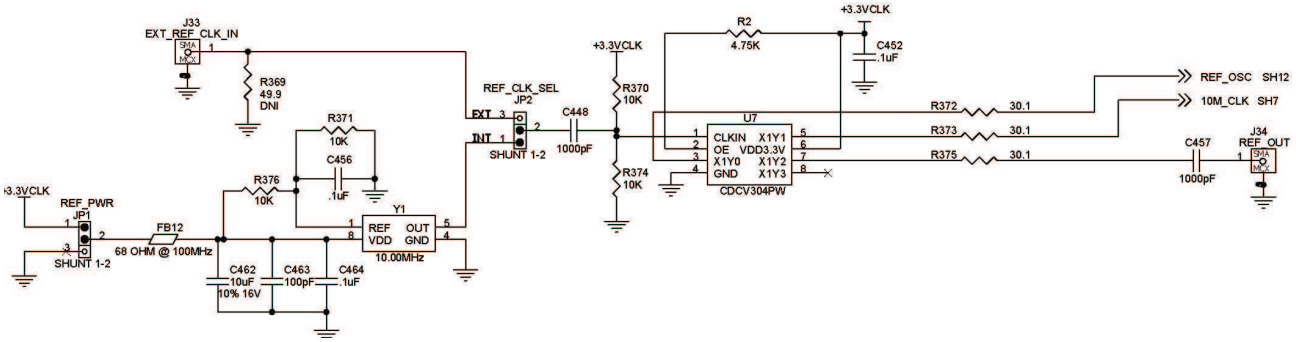
Designator	Description
J8, J24	FPGA Spare I/O's
J22	Power connector to TSW3100
TP1-TP6	Test points for GND
J45	Envelope tracking interface connector (not populated)

A.3 Modifying Board for External VCXO

The VCXO may be converted to external if desired by moving shunts on two jumpers to power off the onboard VCXO.



Remove shunt on SJP16 and SJP17. Add shunt on SJP16 pins 1-2 and shunt SJP17 pins 2-3. An 8-dBm CW can be injected into the J30 MCX connector as the external clock. The CDCM7005 in this case only acts as a buffer and clock divider.



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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 15 VDC to 22 VDC and the output voltage range of 0 VDC to 12 VDC .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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